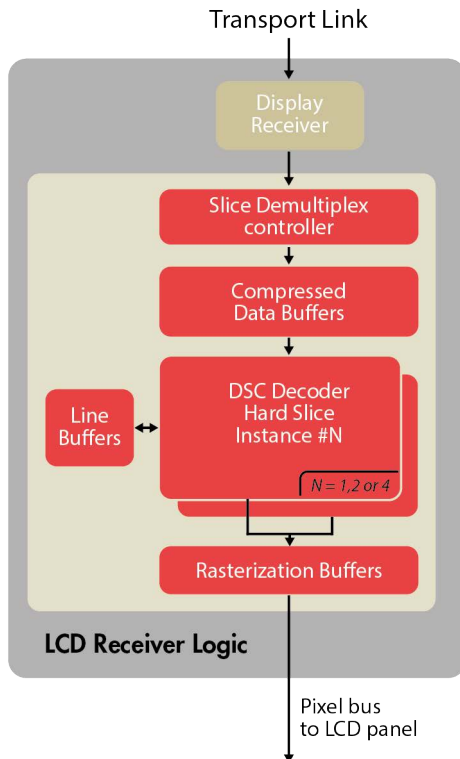


VESA DSC 1.1 Video Decoder IP Core

Applications

- Mobiles
- Tablets
- AR / VR products
- In-car video applications
- Video transmission

Hardent DSC Decoder IP



Hardent provides IP solutions as well as cutting-edge ASIC and FPGA design services for electronics manufacturers using display technology. As a member of VESA and a key contributor of the DSC Task Group, Hardent has used its expertise and skills to develop the very latest standards in display technology. Hardent's high-quality IPs enable clients to accelerate their development schedules and meet demanding time-to-market deadlines.

Key Features

- VESA DSC 1.1 compliant
- Supports all DSC 1.1 mandatory encoding mechanisms
 - MMAP, BP, MPP, and ICH
- Input buffering compatible with transport stream over video interfaces
- Configurable maximum display resolution
 - Up to 4K (4096x2160), 5K (UHD+), and 8K (FUHD)
- 8 and 10 bits per video component
- YCbCr and RGB 4:4:4 video output format
- Resilient to bitstream corruption
- 3 pixels / clock internal processing architecture
- Parameterizable number of parallel slice decoder instances (1, 2 or 4) to adapt to the capability of the technology and target display resolutions used
- Optional DSC features can be disabled to improve area
- 100% verification coverage based on UVM environment
- Verified against the VESA DSC 1.1 C model using a comprehensive test image library

Deliverables

- Encrypted RTL source code IP core
- Functional and structural coverage reports
- Comprehensive integration guide
- Technical support and maintenance updates

Product Options

- IP customization and integration services available on request
- Multi-project licenses available
- UVM verification bindable modules
- FPGA evaluation and prototyping platform



Updated July 2016