Overview

The IPB-SPDIF-AES3 is part of the IPbloq family of Multi-Channel Audio Interfaces, comprising receiver (RX), transmitter (TX) and transceiver (XCVR) IP cores. These IPs can be used in systems on chip for consumer or professional audio applications. Their fully digital design avoid analog PLLs and helps build compact and low-power systems.

Features

- Fully digital IP core
- Pre-synthesis configurable for RX, TX or XCVR configurations
- Supported PCM standards: SPDIF (IEC60958) and AES3
- Supported non-PCM standards: IEC61937, SMPTE 337M
- Encodable formats: AC3, AAC, DTS, MPEG, etc
- Digital clock and data recovery
- Removes stuffing bits in non- PCM mode
- Instantaneous lock on frame preamble
- Minimum system clock frequency 500*Fs
- Front-end: serial audio
- Back-end data interface: I2S, AHB, AXI, AXI Streaming
- Back-end control interface: AHB/APB, AXI, AXI Lite
- Fixed or programmable Channel Status and User Bits information
- Configurable FIFO: RAM size, low and high thresholds
- Programmable Endianness
- Automatic RX sample rate detection.

Benefits

- Eliminates need for a discrete SPDIF-AES3 chips in the BOM
- Supported in both FPGA and ASIC
- Small silicon area and power consumption

Block Diagram

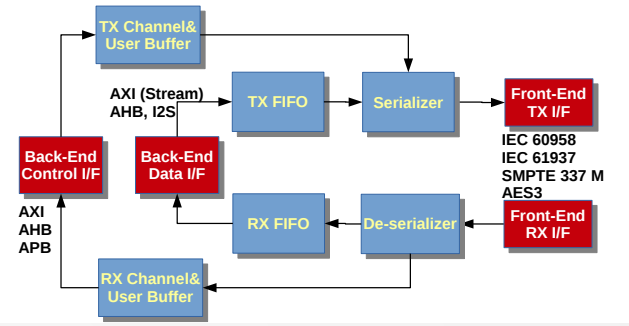

Table 1: Results for Xilinx FPGAs

FPGA	LUTS	FFs	Fmax(MHz)
Spartan-6	2025	1260	100
Kintex-7	1900	1260	133
Virtex-7	1900	1260	150

Table 2: Results for ASIC implementation

TSMC NODE	AREA (mm^2)	Fmax (MHz)
130nm	0.07	200
90nm	0.04	333
65nm	0.02	520

Deliverables

- Datasheet and user documentation for system integration
- RTL code in Verilog or FPGA netlist
- RTL testbench
- Synthesis and implementation constraints

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Disclaimer: IPBloq reserves the right to modify the current technical specifications without notice.