ANALOG BITS

Cut SERDES Power In Half

16/12 FinFET in Production Silicon

7nm Working Silicon Design Kits Available

- 75+ Processes
- 350+ Customers
- 800+ Products

MIXED SIGNAL IP

SERDES
- 1-25G Multi-Protocol
- 3.8mW/Gbps
- 75+ Products
- 10G Wire Bond

PVT SENSORS
- PVT 0.04mm²
- POR 0.02mm²
- Fully integrated
- 190nJ/Measurement

CLOCKS
- 0.02 mm²
- 0.5 µA/MHz
- 100fs RMS Jitter
- 32KHz to 100 MHz X-tal OSC

I/O
- Densest Integration
- 50+ Products
- High Linearity

MEMORY
- 1GHz TCAM
- 30M Transistor
- Cycle-Selectable Operations

Lowest System Cost

Greatest Reliability

Smartest Systems

Corporate Background

Heritage

Focused on differentiated low power mixed-signal IP

- Founded in 1995, based in Silicon Valley
- Independent with no external funding

Track Record

World-class mixed signal CMOS engineering staff

- Extensive experience in advanced SoC designs
- Billions of IP in silicon from 0.25µm to 7nm FF

Core Values

Premier IP partner from architecture to silicon

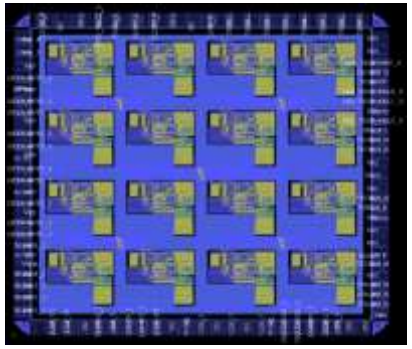
- Customer-centric business engagement
- Engineering-centric support

Client Base

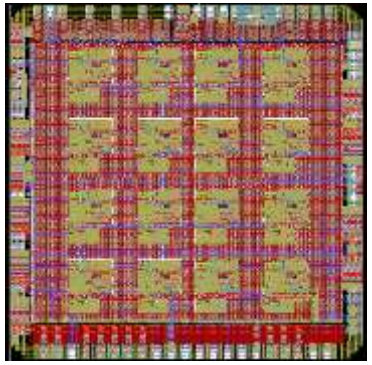
Global customer base - 50% US, 50% international

- 350+ Customers in 70+ Processes

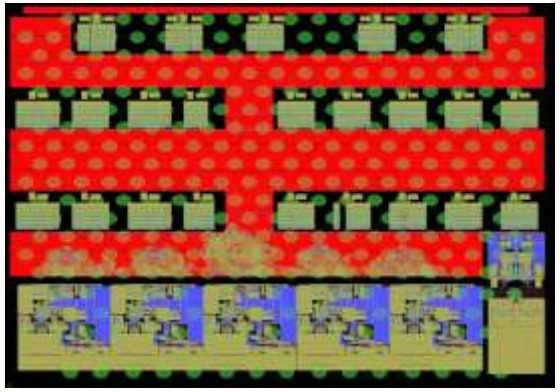
Advanced Technology Leadership
16/12FF IP Shipping in Production and 7nm Pre-Production



16FFC Test Chip



Automotive Grade 16FFC Test Chip



16FFC Multi-Lane SERDES Test Chip

- Multiple products on 16nm/14nm in **Mass Production** for Smart Phones
- Demonstrated **lowest power** 1-16G SERDES test chips in 16FF+
- 16FFC/14LPP test chips with PLL and Sensor, SERDES **Production Silicon**
- 16FFC **Automotive-grade** PLL, Sensor and Xtal OSC test-chip taped-out in August shuttle

- 16FFC 1-25G Enterprise Class SERDES **working silicon demonstrated**
- 16FFC 1-10G Ultra low power SERDES **working silicon demonstrated**
- 7nm FF early partner with TSMC
- 7nm PLL and Sensors **Working Silicon**
- Low Power SERDES Test Chip in 7FF Q4-18
- PCI Gen5 SERDES Q1-19

Qualified Fabs and Processes

70+ Processes and 700+ IP Products Delivered

Merchant Fabs	Process Names (Red in Production, Black pre-production)
tsmc	CL025, CL018G, CL018LV, CL018IMG, CL015G, CL015LV, CL013G, CL013LV CL013LVOD, CL011LV, CL011G, CLN90G, CLN90GT, CLN90LP, CLN80GC, CLN65LP, CLN65GP, CLN55GP, CLN40G, CLN40LP, CLN28HP, CLN28HPL, CLN28HPM, CLN28HPC, CLN28HPC+, CLN20SOC, 16FFT, 16FF+, 16FFC, 12FFC, 7FF, 7FF+
SAMSUNG	45LP, 32LP, 28LP, 28FDSOI, 14LPP, 8LPP, 7LPP
UMC	L250, L180 HS, L150 HS, L130E HS, L130 SP, L130 LL, L90SP, L90G, 65SP, 65LL, 40LP, 28HLP
IBM	7SF, 7SF 8SF, CIMG 8SF, CIMG 9SF, 9LP, 10SF, 10LP, 10LPE, 11LP, 32LP
GLOBALFOUNDRIES	0.13u-Nominal, CH90G, CH90LP, CH65G, CH65LP, CH65LPE, CH45LP, 40LP, 32LP, 28SLP, 22FDSOI, 14FF

IDM Fabs

FUJITSU TOSHIBA

Low Cost Fabs

Dongbu SMIC

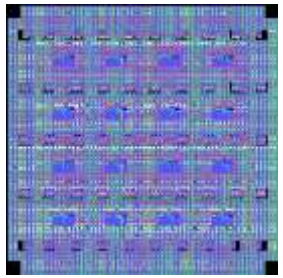
Clocking IP Volume Leader

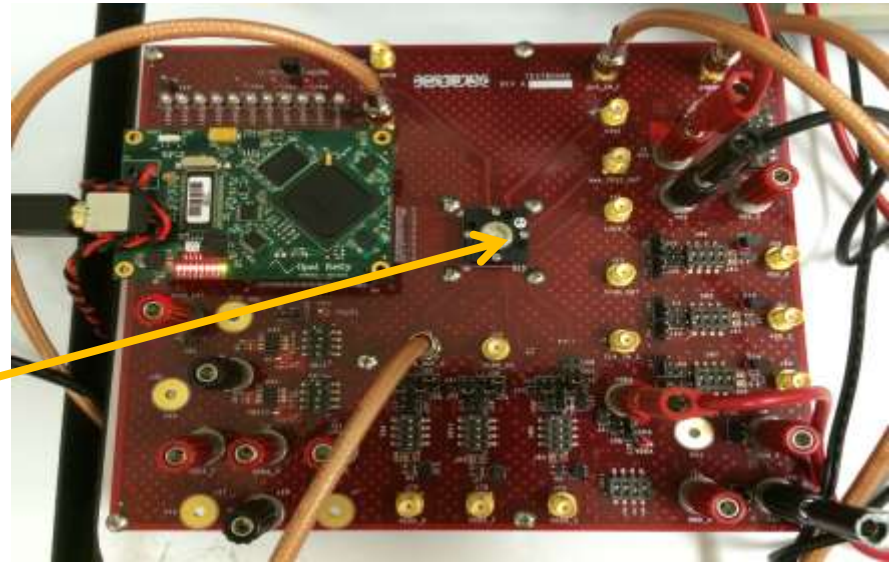
- Industry's broadest and most pervasive clocking IPs

- Wide-range programmable PLL
- High-end Audio / Video Class PLL
  - Fine resolution, Fractional-N, SSCG
- Ultra low jitter sub-picosecond LC PLL
- Ultra low power sub-micro watt IOT class PLL
- High reliability radiation tolerant PLL

10G PLL VCO at 1.25mW on TSMC 7nm Test-Chip

- High Performance Low Power PLL
  - VCO Freq. > 8 GHz (Spec)
  - ***Demo Silicon Data > 10 GHz***
  - Typ Power < 4 mW (Spec)
  - ***Demo Silicon Data < 3mW***
  - Area 0.008 sq.mm





Analog Bits Low-Power, Multi-Protocol SERDES

- Multi-Rate, Multi-Protocol SERDES
  - Lowest power & latency
  - Smallest area
  - Programmable for numerous channel environments

Wearables

- And enabling many SOC applications

FPGA

Consumer Cables

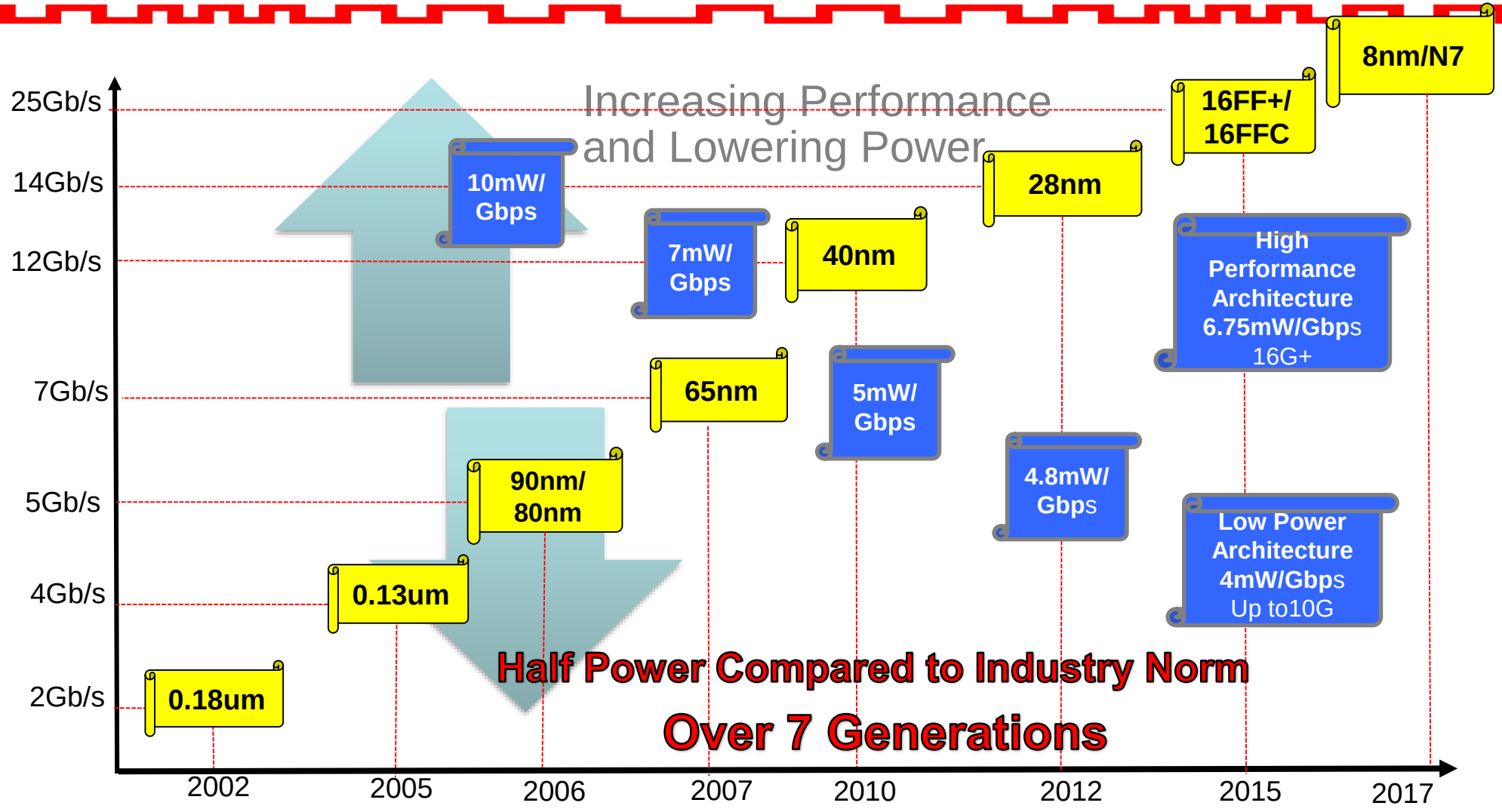
Mobile Computing

DataCenters & Communications

Flat Panel Display

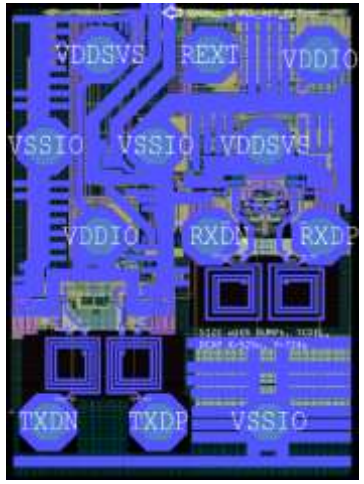
2 Decades of Low Power SERDES Track Record

1st Time Right in over 16 processes including 16/14nm



Unparalleled Power Performance ANALOG BITS

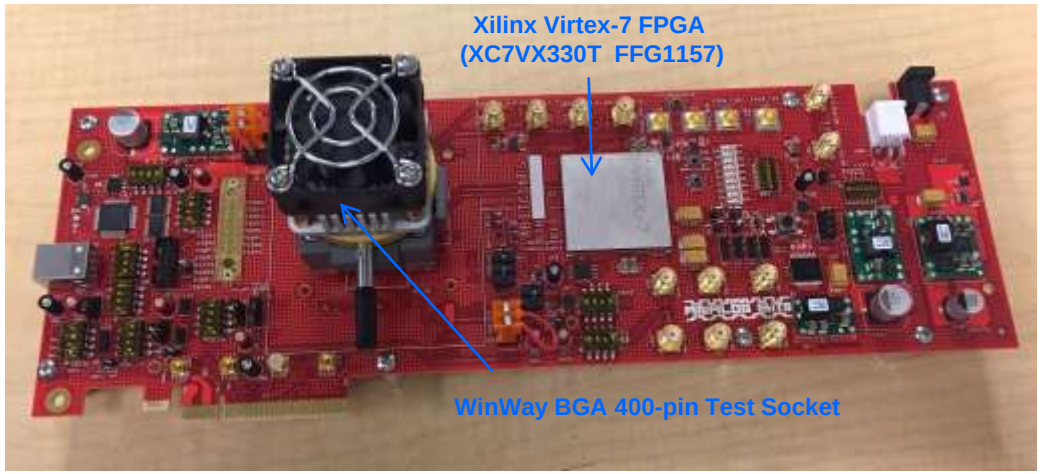
High Performance 1-25G Class SERDES in 16FFC



1-25G Class SERDES PMA

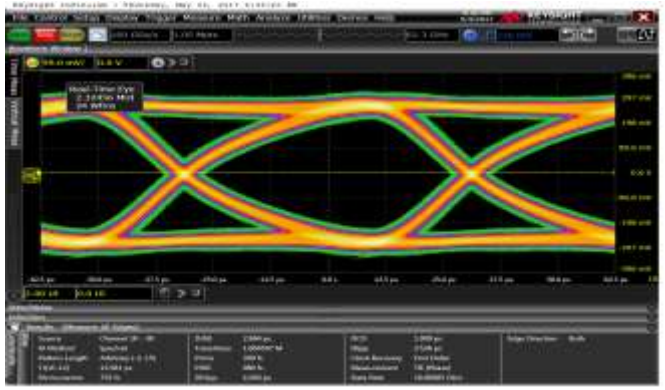
Data Rate (Gbps)	Total Power (mW/lane)	Power (mW/Gbps/lane)
16	98.25	6.9

***Multiprotocol:* XFI,10GKR, PCIe4, SAS4**

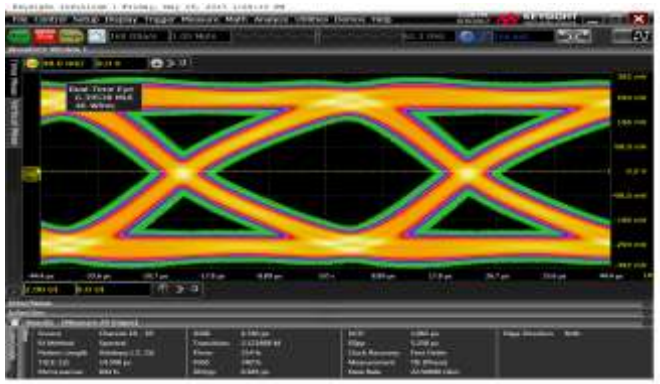


1-25G SERDES Test Board

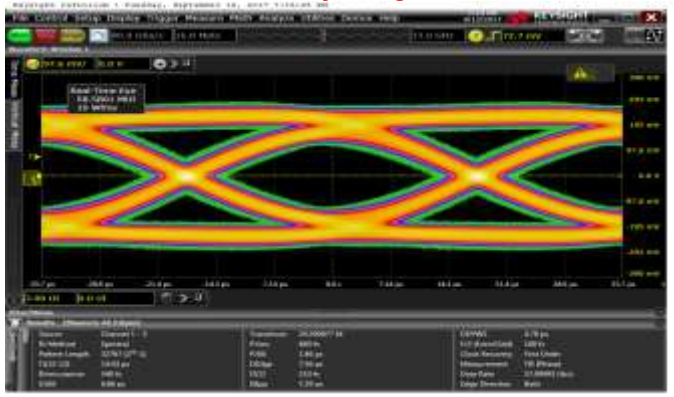
16Gb/s TX Eye Diagram



22.5Gb/s TX Eye Diagram

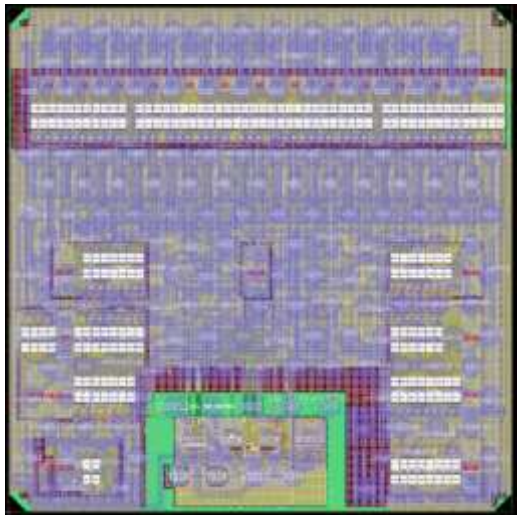


28 Gb/s TX Eye Diagram

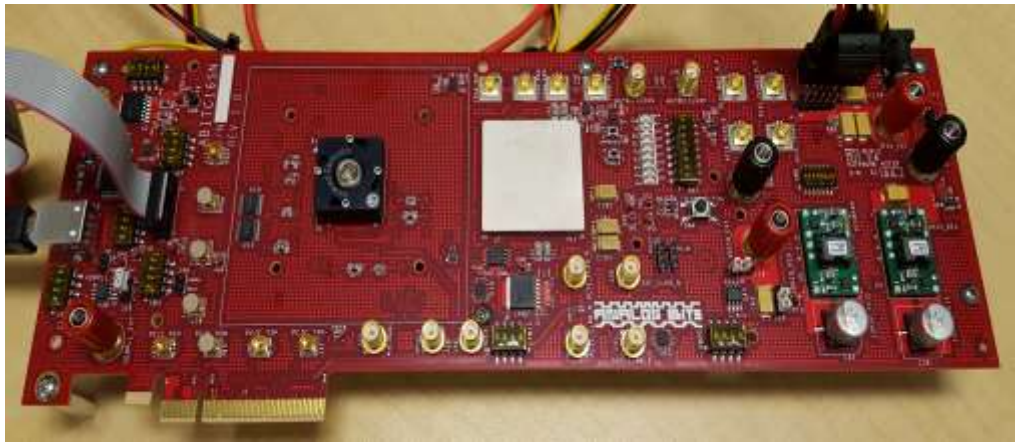


Unparalleled Power Performance ANALOG BITS

Ultra Low Power 1-8G SERDES in 16FFC & 12FFC

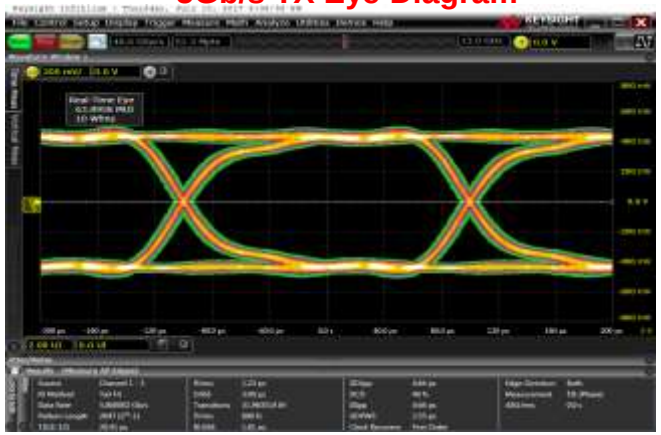


Data Rate (Gbps)	Total Power (mW/lane)	Power (mW/Gbps/lane)
8	34.31	4.29

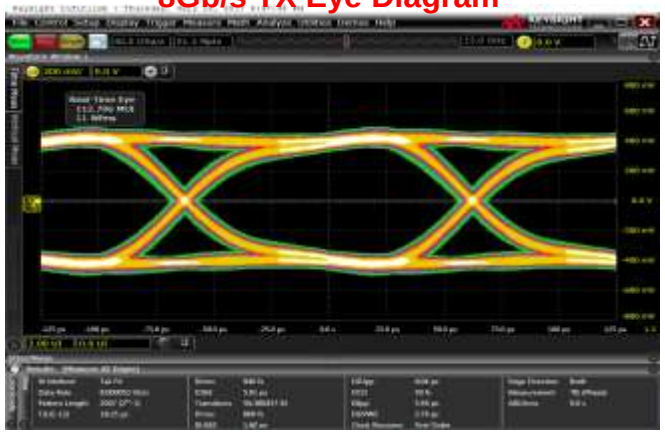


Multiprotocol: SGMII, XAUI/RXAUI, SATA3, PCIe3

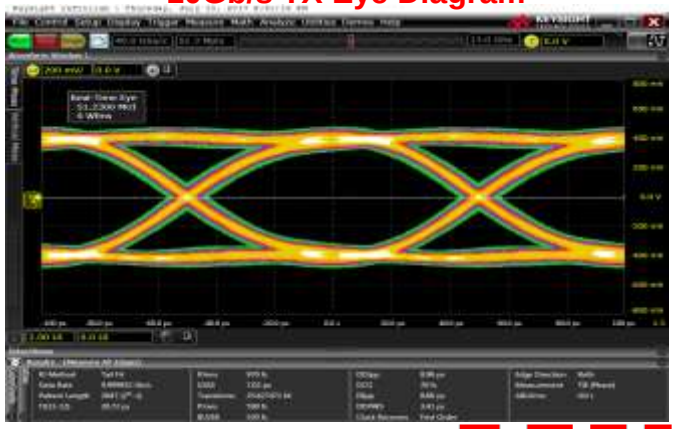
5Gb/s TX Eye Diagram



8Gb/s TX Eye Diagram



10Gb/s TX Eye Diagram



Unparalleled Power Performance ANALOG BITS

Why Analog Bits

Differentiated IP with Broadest Portfolio focused with best in class PPA

Excellent Reputation for Best-in-Class Mixed Signal Designs in Silicon Valley

Global Customer Base from 0.25µm to 7nm FinFET

Business friendly high volume no royalty model