

Overview

The IPB-PNG-E core can be used in systems on chip for encoding picture streams using the Portable Network Graphics (PNG) format. It has been designed for systems requiring high frame rate while encoding RGB images at 24-bit color depth.

Features

- Fully digital IP core
- Supported in FPGA and ASIC
- 24-bit RGB input (R=8, G=8, B=8 bits)
- 800x480 frame size in pixels
- Frame rate: 20 fps
- 256-pixel input/output FIFO
- Input/output simple DMA
- 250kB embedded SRAM
- Simple microprocessor for control and formatting
- Latency: 12.5ms
- Hardware data compressor
- Data compressor simple DMA
- Single processing clock domain
- Accepted user I/O clocks

Benefits

- Achieves high frame rate due to hardware implementation
- Supported in both FPGA and ASIC
- Scalable architecture allows features to be added upon request

Disclaimer: IPBloq reserves the right to modify the current technical specifications without notice.

Block Diagram

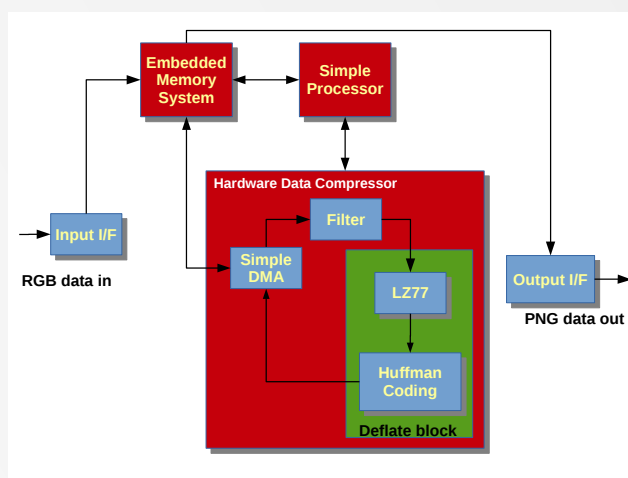


Table 1: Results for Xilinx FPGAs

FPGA	SLICES	BRAM	DSPs
Spartan-6	3500	2 Mbit	10
Kintex-7	3490	2 Mbit	8
Virtex-7	3470	2 Mbit	8

Deliverables

- Datasheet and user documentation for system integration
- RTL code in Verilog or FPGA netlist
- RTL testbench
- Synthesis and implementation constraints

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