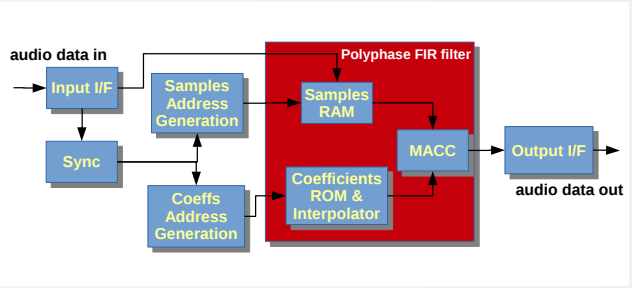
Overview

The IB-ASRC-H is part of the IPbloq family of multi-channel Asynchronous Audio Sample Rate Converters (ASRCs). This IP core can be used in systems on chip for consumer or professional audio applications. It has been designed for systems requiring very high quality in terms of low harmonic distortion and noise, tolerance and rejection of input jitter.

Block Diagram



Features

- Fully digital IP core
- Pre-synthesis configurable up to 8 audio channels
- Automatically adjusts to input and output sample rate changes
- Input and output sample rate range: 8 kHz to 192 kHz
- Sampling rate conversion ratios from 1:7 to 7:1
- Supports multi-channel TDM serial/parallel audio, I2S, AES3/SPDIF
- Tolerates and rejects input jitter
- Latency: $128/FS_{IN} + 2/FS_{OUT}$
- -130 dB THD+N and Dynamic Range
- Reports sample rate conversion ratio in real time
- Fast synchronization time: 128 input sample periods
- Pre-synthesis Clk OUT configuration from $64 \times FS_{OUT}$ to $1024 \times FS_{OUT}$

Table 1: Results for Xilinx FPGAs

FPGA	SLICES	BRAM 9 kb	BRAM 18 kb	BRAM 36 kb	DSPs
Spartan-6	700	0	16	N/A	6
Kintex-7	700	N/A	0	9	4
Virtex-7	650	N/A	0	9	4

Table 2: Results for ASIC implementation

TSMC NODE	CELLS	AREA (mm^2)	Max CLK_IN (MHz)	Max CLK_OUT (MHz)
65nm	9200	0.04	475	200
45nm	9850	0.02	600	275

Benefits

- Eliminates need for a discrete ASRC chip in the BOM
- Supported in both FPGA and ASIC
- Scalable architecture allows features to be added upon request

Deliverables

- Datasheet and user documentation for system integration
- RTL code in Verilog or FPGA netlist
- RTL testbench
- Synthesis and implementation constraints

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Disclaimer: IPBloq reserves the right to modify the current technical specifications without notice.