TFT-LCD-CTRL

TFT/LCD Display Controller

The TFT LCD Controller is a configurable core that provides all the timing control and pixel serialization needed to control TFT LCD Display Panels. The core can also be used with various RAMDACs to interface to VGA Monitors or VGA-style LCD Panels. It interfaces with an AMBA AHB system bus.

The controller supports 24-bit true color and 16-bit high color, as well as an 8-bit color display mode via a 256x24 Pixel Palette. Pixel clock generation, Sync Control, and Display Enable controls are fully programmable and can be used with a wide range of system clock rates.

Display information is held in system memory and is accessed by the core using an internal DMA controller; the core reads from system memory and outputs pixel information to the display. In true color mode, 24-bit pixels are accessed 32 bits at a time. In 16-bit color mode, two 16-bit pixels are accessed 32 bits at a time and then serialized. In 8-bit color mode, four 8-bit pixels are accessed 32 bits at a time and then serialized as 24-bit palette mapped pixels.

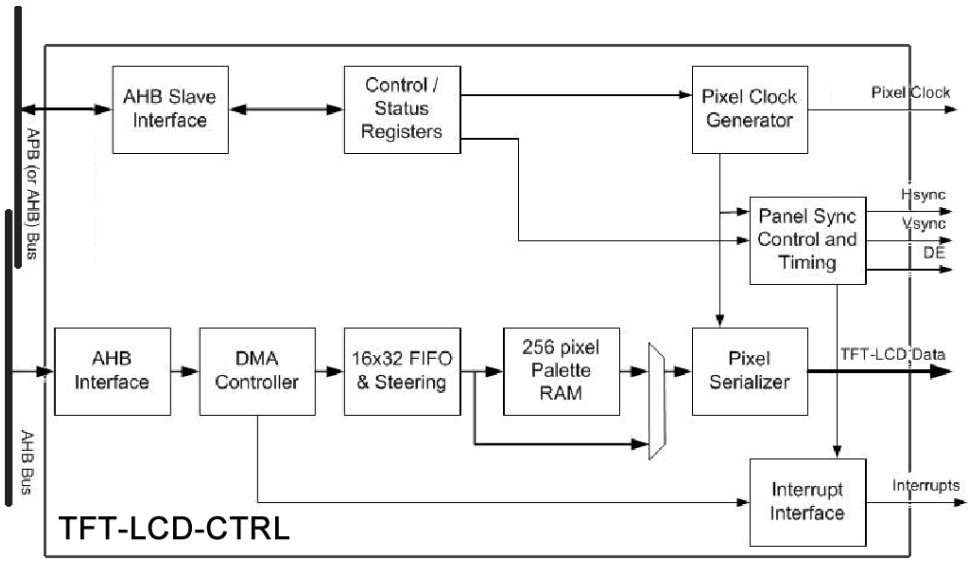
The LCD data interface contains 8-bit Red, 8-bit Green, and 8-bit Blue for a total of 24bits. It will also work with 6-bit RGB panels.

Interrupt sources timed to hsync, vsync, and control signals are programmable and selectable to signal the processor to update display information.

Support

The TFT-LCD-CTRL as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Block Diagram



Features

Display Panel Support

- 24-bit and 16-bit LCD or TFT panels
- Programmable display resolution
- Programmable display timing:
  - Front/Back porch
  - Sync pulses width
- Flexible pixel clock generation
  - Via clock divider from AHB bus clock
  - From dedicated pixel-clock pin

Source Color Formats

- True color: 24-bit pixel
- High Color: 16-bit pixel
- 8-bit color (RGB332)

System Interfaces

- AHB Slave for control/status register controls and color palette
- AHB (DMA-capable) Master for pixel data, feeding a 15x32 Pixel FIFO
- Configurable interrupts

Deliverables

- Verilog RTL source code or targeted netlist for Altera, Microsemi, or Xilinx
- Simulation testbench and comprehensive documentation

Maturity

- Multiple times production proven in ASICs and FPGAs

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March 2016