QSPI-XIP-AHB

Quad SPI Bus Controller with XIP, for AHB

The QSPI-XIP-AHB core implements a quad Serial Peripheral Interface (SPI) module that either controls a serial data link as a master, or reacts to a serial data link as a slave.

Users can configure the core via software control to be a master or slave device. In master mode, it can be used with up to four SPI slave devices.

Reading and writing the core is done on the AMBA® AHB bus interface. The core operates in various data modes from 4 to 32 bits (eight modes are supported in multiples of four data bits). The data is then serialized and transmitted, either LSB or MSB first, using the standard four-wire SPI bus interface or the extended Dual or Quad Bus modes.

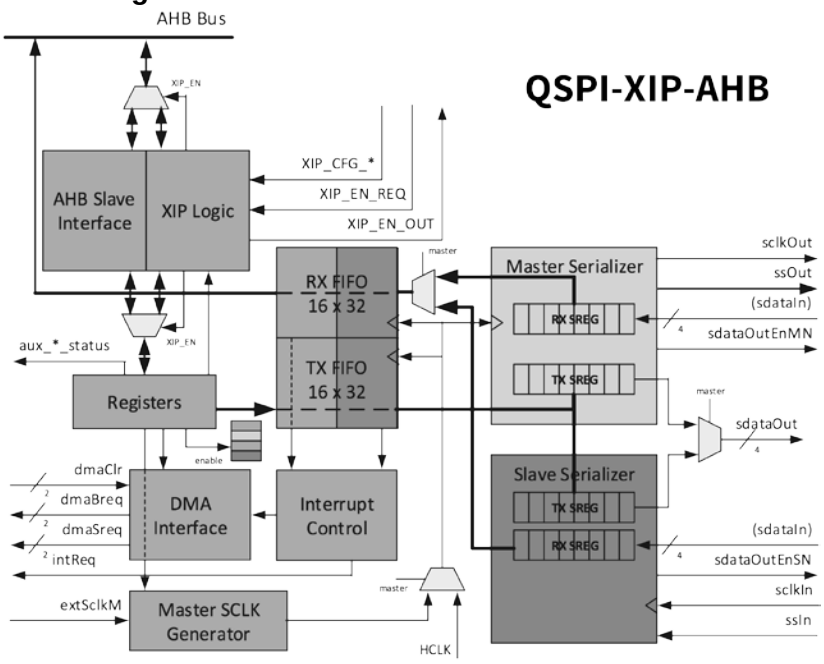
The QSPI-XIP-AHB core is compatible with various industry-standard DMA controllers. Enabling DMA operation assists a DMA controller in the loading (writing) of the transmit FIFO, and the unloading (reading) of the receive FIFO.

The Execute in Place (XIP) Mode allows an AHB Master to directly read the contents of any of several industry-standard flash devices (such as Winbond, Macronix, Spansion, and Micron devices) simply by reading from the address space of the QSPI Controller.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Block Diagram



Features

- Controls high-speed, synchronous, serial communication
  - Motorola Serial Peripheral Interface (SPI) format support
  - TI Synchronous Serial Frame format support
- Master or Slave mode; controls up to four slaves in Master mode
  - Separate SCLK input for Master Mode
  - Asynchronous Slave Interface
- Single, Dual and Quad-bit modes
- Full duplex operation; half-duplex support
- Compatible with many industry-standard serial Flash devices
  - Execute in Place (XIP) mode
- AMBA® AHB interface
- DMA Interface
- 4-bit to 32-bit serial TX/RX
- 8 to 256 word TX/RX FIFO, configurable
- Interrupt control
- LSB or MSB mode
- National Microwire Frame format support
- XIP feature can optionally be removed

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