OSPI-XIP-AHB

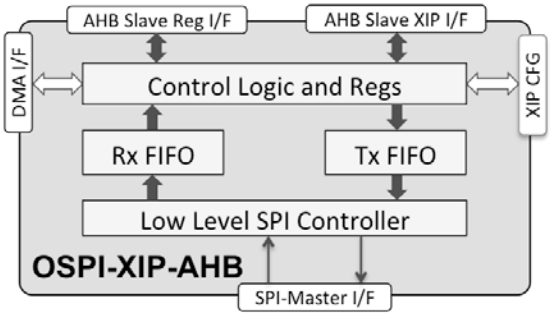
Single, Dual, Quad, & Octal SPI Flash Controller for AHB

The OSPI-XIP-AHB core is a flexible, high-performance, SPI Flash memory controller. It enables AHB bus masters (e.g. host processors or DMA engines) to access the Flash memory address space using standard AMBA AHB 2.0 transactions, without any software assistance. Furthermore, the controller core is able to exploit the bandwidth that standard and high-performance SPI Flash devices offer.

The controller provides two 32-bit AHB slave interfaces towards the on-chip system, and acts as a master on an SPI bus that can accept up to four slave devices. The first AHB slave interface supports eXecute-In-Place (XIP), meaning that the core acts as an AHB-to-SPI bridge for read transfers. The second AHB slave interface provides access to the core's control and status registers. The register interface enables low-level control of the SPI master port, enabling the system to perform read or write transactions over the SPI bus.

A sideband DMA signaling port can optionally be used to optimize the data transfers between an AHB master and the OSPI-XIP-AHB core. The core also provides a dedicated interface that can be used to control the XIP mode parameters. This XIP configuration interface can be hardwired or driven by other logic, and enables XIP right after reset and without any programming of the core registers.

Block Diagram



The OSPI-XIP-AHB can efficiently utilize the bandwidth of standard and high-performance SPI Flash devices. It supports single transfer rate (STR) or dual transfer rate (DTR) over single, dual, quad, or octal data lines. The SPI link parameters—such as clock phase and polarity, and the bit-width of SPI transmissions—are fully programmable to ensure operations in all widely used SPI bus configurations. Moreover, the core supports the de-facto standard for the encoding of Flash access commends and allows run-time configuration of the command parameters, enabling operation with Flash devices from all major vendors, including Macronix, Micron, Spansion, and Windbond.

This core has been designed with industry best practices, and its reliability and low risk have been proven through both rigorous verification and customer production.

Features

SPI Flash memory controller supporting XIP and STR or DTR over single, dual, quad, and octal links. XIP feature can optionally be removed.

System Interfaces

- 32-bit AHB Slave for Register Access
- 32-bit AHB Slave Execute-in-Place (XIP) for direct bridging of AHB to SPI
- Interrupt line
- Sideband DMA interface, for easy integration with external DMA controller
- XIP configuration pins, enabling use of XIP mode after reset and without prior programming

SPI Master Interface

- Single, Dual, Quad, and Octal data lines
- Single Transfer Rate (STR) or Dual Transfer Rate (DTR)
- 4, 8, 16, or 32 bit word transmissions per SPI data line
- Full and Half Duplex operation
- Up to four SPI slaves
- Programmable serial clock polarity and phase
- Serial clock is provided by the system, and is totally independent from the AHB clock

Flash Devices Support for XIP

- Supports de-facto standard for Flash command encoding and all widely used SPI bus configurations
- Supports Flash devices from all major vendors, including Macronix, Micron, Spansion and Windbond

Deliverables

- Verilog RTL source coder or targeted FPGA netlist
- User Documentation
- Testbench and sample synthesis

Applications

The OSPI-XIP-AHB can be used in SoC designs storing firmware and or application data to an external SPI Flash device, and that are using an AHB, or AHB-Lite SoC bus.

Related IP Cores

The OSPI-XIP-AHB is part of a group of available AMBA peripheral cores that includes bus infrastructure cores, bus bridges, interface controllers (SPI, I2C, CAN, UARTs, and LIN), timers, a real-time clock, and more.

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