LIN

LIN Bus Master / Slave Controller

The LIN core is a communication controller that transmits and receives complete LIN frames to perform serial communication according to the LIN Protocol Specification. The LIN controller can be implemented as a master or as a slave and operate on LIN 1.3, 2.0, 2.1 or 2.2 LIN network. It uses a single master/multiple slave concept for message transfer between nodes of the LIN network. The message transfer can be controlled via a micro controller interface and a LIN transceiver is needed for the connection to the LIN bus.

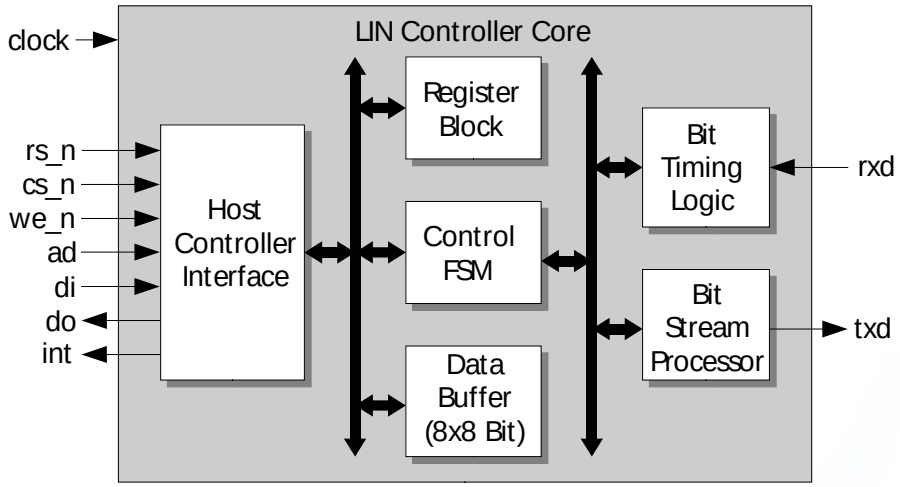
The LIN core is a microcode-free design developed for reuse in ASIC and FPGA implementations. The scan-ready design is strictly synchronous with positive-edge clocking and no internal tri-states. The robustly verified core has been production proven multiple times.

Applications

The LIN core can be utilized for a variety of applications including;

- low cost automotive networks
- interfaces for sensors and actuators

Block Diagram



Features

- Support of LIN specification 2.0, 2.1, and 2.2A
  - Backwards compatible with LIN specification 1.3
- Configurable for support of master or slave functionality
- Programmable data rate between 1 Kbit/s and 20 Kbit/s (for master)
- Automatic bit rate detection (for slave)
- 8-byte data buffer
- 8-bit host controller interface
  - Wrappers for 32bit busses (e.g. APB) can be made available upon request
- Slave can be implemented with or without clock synchronization
- Fully synchronous design, available in VHDL or Verilog, completely synthesizable
- The LIN Controller synthesizes to approximate 2500 to 3800 gates depending on the configuration
- Robustly verified and multiple times production proven IP core

Functional Description

The LIN core is partitioned into modules as shown in the block diagram.

Host Controller Interface

This interface is responsible for handling the communication with the host controller of the system.

Register Block

The Register Block provides control registers and status registers to control the LIN message transfer. Access to the registers is possible via the host controller interface.

Data Buffer

The 8-byte Data Buffer stores the data that has to be sent with the current LIN frame or the data that has been received with the last LIN frame. Access to the Data Buffer is possible via the host controller interface.

Control FSM

The finite control state machine is responsible for the behavior of the core depending on host controller commands and bus activity. It generates and processes the LIN frame fields according to the LIN protocol.

Bit Stream Processor

This module converts the data stream from parallel to serial (from transmit buffer to bus) and from serial to parallel (from bus to receive buffer).

Bit Timing Logic

The Bit Timing Logic is responsible for synchronizing the received data stream from the bus with the internal bit time clock.

Implementation Results

LIN reference designs have been evaluated in a variety of technologies. The following are sample ASIC results.

ASIC Technology	Configuration	Approx. Area	Frequency[1]
TSMC 0.18	Master	2,710 gates	4 MHz
TSMC 0.18	Slave	3,840 gates	4 MHz
TSMC 0.18	Slave w/ auto bit rate	4,060 gates	4 MHz
TSMC 0.13	Master	2,500 gates	4 MHz
TSMC 0.13	Slave	3,500 gates	4 MHz
TSMC 0.13	Slave w/ auto bit rate	3,760 gates	4 MHz

[1] 4 MHz is the required LIN speed

Core Modifications

The LIN core can be modified to include an acceptance filter. With that, a simple LIN slave that transmits response frames for only one identifier could be realized without the assistance of a host controller.

Please contact CAST, Inc. directly for any required modifications.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements

Deliverables

The core includes everything required for successful implementation:

- VHDL or Verilog RTL source code
- Post-synthesis EDIF (netlist licenses)
- Testbench
- Vectors for testbench
- Simulation and synthesis script
- Expected results for testbench

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