I2C-SMBUS

I2C & SMBus Controller Core

The I2C-SMBUS core implements a serial interface controller for the Inter-Integrated Circuit (I2C) bus and the latest specification of the System Management Bus (SMBus).

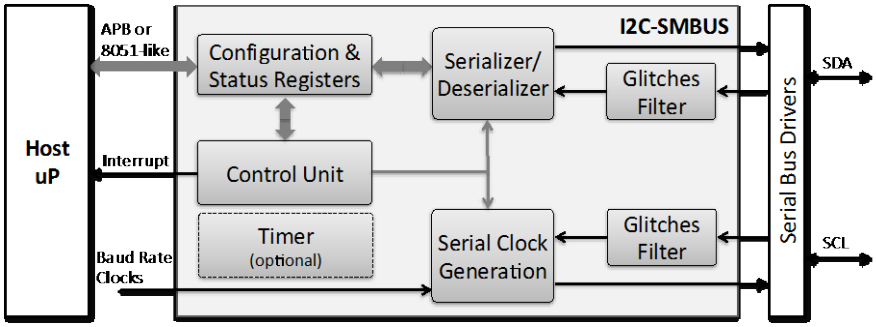
The core can be programmed to operate either as a bus master or a slave, and it is easy to program and integrate. An arbitration mechanism allows operation in a multiple master bus and the SMBus provisioned clock synchronization mechanism allows fast-master/slow-slave communication. Furthermore, the core detects timeout and errors to prevent bus deadlocks, and can filter out glitches on the serial line. The control, status, and data registers of the I2C-SMBUS core are accessible via an AMBA APB or a generic memory mapped interface.

The I2C-SMBUS is a microcode-free design developed for reuse in ASIC and FPGA implementations. The design uses rising-edge-triggered flip-flops only with the reset type (i.e. asynchronous and/or synchronous) being configurable at synthesis time. Furthermore, the core does not use tri-states; therefore scan insertion is straightforward.

Applications

The I2C-SMBUS can manage the communication of a host processor with peripherals such as sensors, smart battery subsystems, analog front ends, analog-to-digital and digital to analog converters, and display controllers.

Block Diagram



Implementation Results

I2C-SMBUS core reference designs have been evaluated in a variety of technologies. The following are sample implementation results.

Technology	I2C-SMBUS (w/o Timer) Area	Timer Area	Core/Bus Clock Frequency
TSMC 90nm process	1,650 gates	600 gates	100 MHz
TSMC 40nm process	1,900 gates	700 gates	100 MHz

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Features

Standards Compliance

- Phillips I2C
- SMBus Version 2.0 & 3.0

Operation Modes

- Master Transmitter Mode
- Master Receiver Mode
- Slave Receiver Mode
- Slave Transmitter Mode

Functionality

- Seven-bit Addressing
- Byte-wide Transfers
- Bus Arbitration
- Clock signal (SCL) generation (in master mode) and data synchronization
- START/STOP Timing detection and generation
- Timeout/Bus error detection
- Clock-Low Extension to allow fast-master slow-slave communication
- Configurable glitches filter for clock and data serial lines
- Bus status reporting

Interfaces

- I2C–SMBUS
  - A pair of unidirectional signals for SCL and SDA
  - Control for the serial line buffers/drivers
- Host
  - 32-bit APB or 8-bit generic (8051-like) for register access
  - Interrupt line
- Clocks
  - Core operates on the host-interface clock
  - Reference clock signals used to generate the serial clock (SCL)

Deliverables

- RTL source code or targeted FPGA netlist
- Testbench
- Sample simulation and synthesis script
- Extensive documentation
- Sample SMBUS software driver

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