EMAC-1G

Gigabit Ethernet Media Access Controller Core

Implements an Ethernet Media Access Controller compatible with the 10/100 Mbps IEEE 802.3 and 1Gbps IEEE 802.3-2002 specifications. The controller provides half- or full-duplex operation, supports jumbo frames, and optionally provides a reach set of statistics counters enabling station management.

A host processor can control the operation of the core via a slave interface that provides access to its control and status registers. The EMAC-1G features two master ports for data transfers, one for transmit and one for receive. The two DMA engines use buffer descriptors to automatically transfer data from local FIFOs to an external shared memory. The core supports 32-bit AMBA/AHB or Wishbone SoC buses; other bus interfaces are available on request.
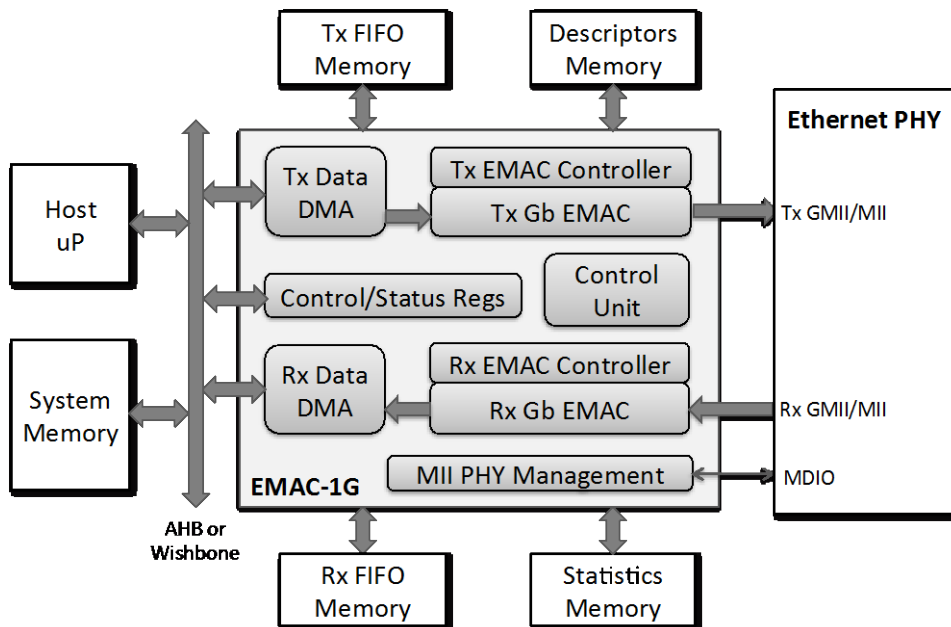
Integration with an Ethernet PHY is straightforward, as the controller core supports the Media Independent Interface (MII) and the Gigabit Media Independent Interface (GMII) physical layer interface standards.

The EMAC-1G is production proven in ASIC and FPGA technologies.

Applications

The EMAC-1G can be used tin any SoC design requiring Ethernet connectivity.

Block Diagram

Implementation Results

Technology	Frequency (MHz)	Eq. NAND2 Gates
TSMC 40nm G	25	28,352
	50	28,352
	125	28,354
TSMC 65nm LP	25	29,013
	50	29,013
	125	29,027
TSMC 65nm GP	25	27,068
	50	27,068
	125	27,069
TSMC 90nm G	25	25,015
	50	25,017
	125	25,024
SMIC 130nm	25	24,853
	50	24,872
	125	25,412

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in Verilog RTL or as targeted FPGA netlist, and its deliverables include everything required for a successful implementation, including an extensive testbench, comprehensive documentation and a sample Linux driver.