C82380

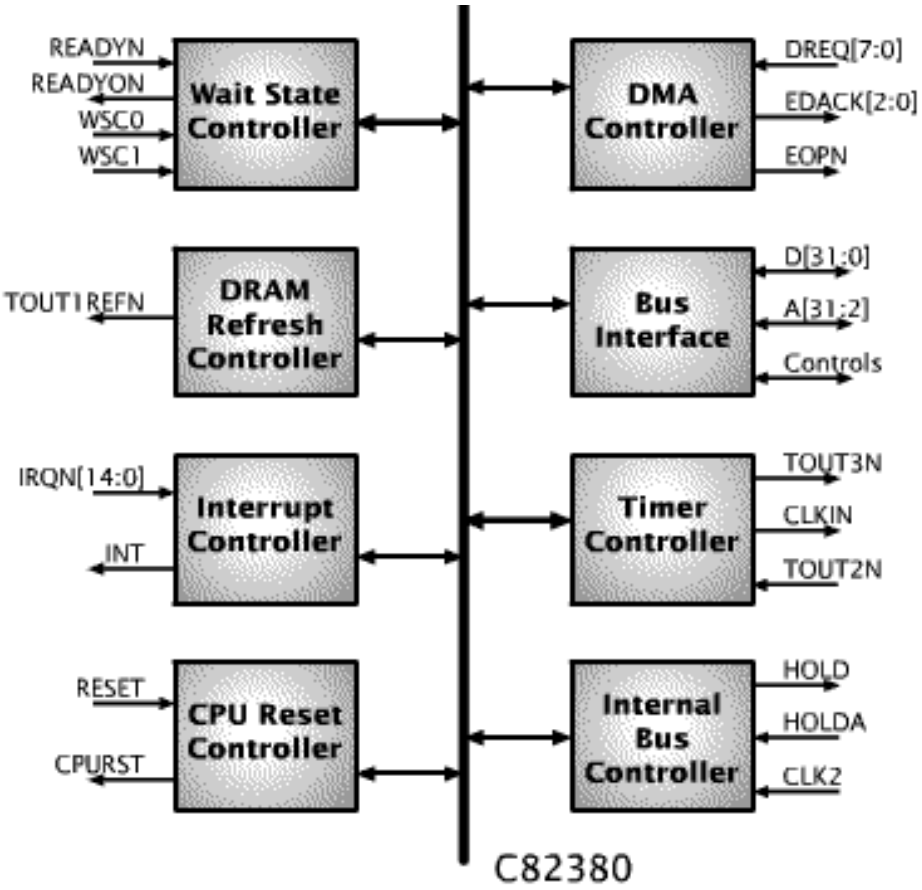
32-Bit DMA Controller with Integrated Support Peripherals Core

The C82380 32-Bit DMA Controller core is a multi-function support system. It is designed to provide peripheral support such as Interrupt, DRAM, DMA, Timer and other Controls for the 80386 bus environment. The integrated control allows simplified programming of all peripherals.

Applications

The C82380 core is used as the peripheral set for 80386 based systems.

Block Diagram



Features

- Eight independently programmable channels of 32-Bit DMA
- Twenty source, individually programmable Interrupt channels
  - Fifteen external interrupts
  - 5 internal interrupts
  - Intel 8259 superset
- Four 16-Bit Programmable Interval Timers
  - Intel 8254 compatible
- Programmable Wait State generator
  - 0 to 15 Wait states Pipelined
  - 1 to 16 Wait states Non-Pipelined
- DRAM Refresh Controller
- The C82380 is available in VHDL and Verilog.
- Functionally based on the Intel 82380 device

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Functional Description

The C82380 core is partitioned into modules as shown in the block diagram and described below:

Internal Bus Controller

This module is used to arbitrate for bus control using the **hold** and **hold acknowledge** signals.

Wait State Controller

The function of this block is to generate the **ready** signal. It is programmable allowing any peripheral that requires wait states to create them.

DRAM Refresh Controller

This block creates the signal required by Dynamic RAMs to start their refresh cycle.

Interrupt Controller

This block functions like an Intel 8259 Interrupt Controller. It is fully programmable and capable of servicing 15 interrupt lines (which can be connected to 15 slave Interrupt Controllers allowing up to 120 interrupts in total).

CPU Reset Controller

This block controls the reset line for the CPU. It can be controlled through software or hardware.

DMA Controller

This block is the heart of the C82380. It is a 32 Bit DMA Controller with 8 channels each individually programmable.

Bus Interface

This block is the interface between the system and the C82380. All address, data and control signals from and to the CPU are controlled by it.

Timer Controller

This block is functionally equivalent to an expanded Intel 8254 Interval Timer. One timer is used internally leaving 3 timers accessible to the developer.

Core Modifications

The C82380 core can be customized to include a greater number of interrupts, timer channels and DMA channels. If required, functions can be removed as well. Please contact CAST for any required modifications.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The C82380 DMA Controller core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 82380 chip, and the results compared with the core's simulation outputs.

Deliverables

The core includes everything required for successful implementation:

- HDL RTL source code
- Sophisticated self-checking HDL Testbench including everything needed to test the core
- Simulation scripts, vectors, and expected results
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide

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